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Deliverable D4.1
RFET Circuit Elements Exploiting Inherent Higher Functionality

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Document Abstract

In this deliverable we present our findings for **analog circuits** benefitting from the **inherent higher functionality** provided by Reconfigurable Field Effect Transistors (RFETs). For this purpose, we first give a brief introduction to the **transistor models** available for analog circuit modelling. The DC-models provided by the project partners were analyzed to gain a better understanding of transistor behavior and to find useful operating regions. Subsequently circuit elements that exploit the inherited functional behavior of the devices were simulated. Since the modelling is still in active development at the time of submitting this deliverable certain aspects are not finalized. The current model limitations are analyzed and our approach in improving model stability and usability is described.

In the second part of the deliverable we present simple **circuit blocks based on RFETs**. The reason for starting our analysis with common standard integrated circuit building blocks instead of more complex circuits is that most complex integrated circuits are mostly an extension and clever combination of these standard circuit building blocks, like current mirrors, differential input stages, diode and common-source circuits and more. Further beneficial circuit blocks include an RFET based transmission gate and the single device mixer circuit. They serve as foundational tools for developing more advanced and complex circuit designs in the future.

Table of Content

1. Introduction

This document presents the findings of our investigation into the behavior and application possibilities of modified standard circuits for the use of Reconfigurable Field Effect Transistor (RFET) devices. Since device modeling for analog circuit simulation of RFETs is still in active and early development, section 2 will explore the possibilities and limits of the current available models as well as possible suggestions for improvements. Our focus hereby was to find models to explore ideas for suitable circuits and feedback for possible model improvement from a circuit designer perspective.

Section 3 starts with an introduction to the RFET as circuit element. Furthermore, we present our findings of fundamental, integrated analog circuit building blocks exhibiting additional functionality by the employment of RFETs. These findings highlight the versatility of RFETs in enabling novel design paradigms.

2. RFET Model Overview

At the time of writing this deliverable, no SPICE-compatible closed form compact model was available for RFET in literature. While several other RFET models in different technologies are already available for circuit design, all are still in ongoing development. All RFET models currently available to the SENSOTERIC project partners are listed in Table 1. The models have a variety of architectures. Most models use tables of simulation or measurement data and read them by either a Verilog-A code or via an AI model. Table models are very efficient to use as they are easy to generate, have predictable behavior and fit the input data well if the input data density is high enough. In addition, a first formula-based model developed in WP2 is currently under evaluation. Currently all models include DC and rudimentary AC behavior but lack noise models. However, this is sufficient to start designing circuits and evaluate the inherent functionality of the RFETs.

Table 1: RFET models available to SENSOTERIC project partners at M12.

Model / Technology (Partner)	Status / Limits	Architecture
TIG-RFET 90nm SOI Based AI Model [1] (TUW)	DC model, limited accuracy, high threshold voltages, non-symmetrical	Predictive AI model
TIG-RFET 14nm GeRFET [2] (NLB)	DC model, AC unrealistic, Germanium based	Predictive Table model
BB-RFET 22nm FDSOI [3] (NLB)	DC and AC, under evaluation	Table model
TIG-RFET 22nm FDSOI [4] (NLB)	DC and AC, under evaluation	Predictive Table model
DIG-RFET 200 nm SPICE model (UBx)	DC and AC, under evaluation	Formula based
Preliminary NDR GeRFET Table model (TUDa & TUW)	Under development, based on measured device data (not simulated), not fully characterized (missing data points), temperature data available	Table model, AI model (planned)

1. *Limitations of* Table *Models*

While the models behaved as intended in most cases, we also run into unwanted behavior during extensive use. While this is not the focus of this deliverable, we still want to mention the identified problems and solutions since they are necessary for working circuit simulation.

Care must be taken when working with noise in the simulation or measurement used to generate data for the table models as it can drastically affect the stability of circuit simulations. For example, we found that noise in the measurements of the low current region of the GeRFET table model, comparable to the cut-off region in a traditional MOSFET, sometimes resulted in the drain current flowing in the opposite direction of the V_{DS} potential. This caused unrealistic voltage spikes or operating points outside of reasonable regions when performing analog circuit simulations in Cadence Virtuoso. As the noise was only relevant in the low current region, the error in the simulations could be corrected by changing the sign of the noise current in the expected direction. While this of course introduces a small deviation from the simulated model data we expect that this is a simulation artifact from generating the data. The same would hold true in case of very small currents close to the resolution limit of the system when measurement data would be used for model generation.

Another point to mention is the sorting of the table data, which can drastically speed up the simulations in Cadence Virtuoso by more than 200% for a single transistor circuit. The data in the table needs to be sorted with the slowest changing variable at the left most column, then second slowest changing one and so on, to efficiently be used by Verilog-A *$table_model* function. While other orderings also seem to work, they significantly decrease performance in the analog simulator. It is important to state that this may only hold true for Cadence Virtuoso as other implementations may need a different sorting.

The Ge RFET table models was used a baseline model to be referred to the Ge-RFET NDR technology developed currently in WP2. An extension of this model is currently developed to include NDR effects. The other table models listed in Table 1 are more recent models aligned to the 22nm FDSOI technology and are therefore still under evaluation for their limits. In the simulations we performed we could see as expected a similar general behavior to the GeRFET model. Therefore, all findings presented in this document, which were generated utilizing the GeRFET model should also hold true for the other models.

2. *AI and Compact Models*

An alternative to direct table models are AI models, which have already been developed and used by [1]. They can be easily fitted to simulation or measurement data [5] and offer a high degree of flexibility in model complexity. In addition, because the AI models are augmented with noise to learn more efficiently, the noise in the training data does not have a large effect on the output of the model. This makes this implementation more robust to current noise in the training data. The augmentation with current noise results in a smoothed output of the model, which is desirable to support fast convergence of circuit simulations. While this is of course a very promising modeling approach it is very reliant on the quality of the learning data used for model generation. The first iteration listed in Table 1 was based on data generated by older generations TCAD models, which were not yet optimized for use in analog circuits. Iterations more related to the 22nm technology are currently under evaluation [5].

In the future, we hope to extend this exploration to AC and noise behavior to further exploit the inherent functionality of RFETs and build more complex circuit based on the circuit blocks shown in this deliverable. In addition, we are looking forward to use formula-based models currently developed on WP3. Also, having formulas at hand can be useful in circuit design, based on hand calculations or spreadsheets.

3. RFET Circuit Elements

In the search for novel circuit elements, we have analyzed standard integrated circuit blocks. These circuits have in common that they are composed of a small number of transistors and fulfil a basic function. We focused mostly on elementary circuits that in most cases only consist of 2 transistors. While this seems to be a low number of transistors, a surprising number of useful circuits can be formed. To give a good overview

over the versatility of basic 2 transistor CMOS circuits we can recommend the reading of "*Fifty Nifty Variations of Two Transistor Circuits*" [6].

RFETs offer the circuit designer two kinds of advantages over traditional n-/p-FET devices: reconfigurability and tunability. Full reconfigurability refers to switching the transistor behavior from n-channel to p-channel by changing the majority carriers inside the device channel, while tunability refers to the inherent change in conductivity by modulating the available number of majority carriers. In this deliverable, we have focused on the tunability aspects of circuits, which have many applications when RFETs are incorporated into traditional standard circuits. For the following circuit demonstration exploiting the inherent higher functionality of RFETs, the GeRFET model has been primarily used. However, the circuits described can generally be implemented by any RFET technology.

1. *RFET Symbol*

Figure 1: Symbol of a 2-Gate RFET.

In this deliverable, all circuits are designed with three-gated RFET variants, also connecting the two outer gates together. While in most cases this arrangement of the RFET is completely symmetrical, in design it is helpful from a design perspective to define a source and drain contact. Fig. 1 shows our preferred symbol for this RFET. It consists of a program gate (PG), control gate (CG), a drain (D) and a source (S) terminal. When utilizing the RFET we tend to use the source as either the lowest potential when used as an n-channel device or as the highest potential, when configured as p-channel device as this helps to establish a design similar to conventional CMOS circuits. This will not be possible in every circuit when utilizing dynamic polarity control.

By changing the potential of the programming gate, we can choose the kind and amount of majority carriers that can enter the channel. Therefore, the type of the device can be set at runtime. The control gate influences how well the channel conducts these charges, but the highest current I_D is limited to the number of available charges injected by the source and drain gates. Since both gates allow the behaviour of the device to be changed post-fabrication, it is possible to massively change the device characteristics at runtime, which is the main premise we explore in this deliverable.

2. *RFET* Diode *Circuits*

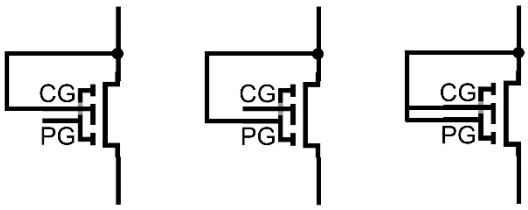

Figure 2: RFET Diode configurations: V_{PG} variable (left), V_{CG} variable (center), not variable (right).

RFETs offer an advantage over classical CMOS technology due to their tunability. Additionally, in the context of diode circuits, RFETs provide a secondary benefit: they can be configured in multiple ways by the circuit designer, offering greater flexibility and versatility.

For a classic CMOS diode connection, a designer would connect gate to drain. Since this RFET variant has two independently accessible gates the question arises which one should be connected to the drain and what is the behavioral difference between the three possible choices as depicted in Figure 2. These choices either have the control or programming gate connected to the drain, while leaving the other gate free to apply a bias voltage. There is also the third possibility to connect both gates to the drain, which simplifies the design but also removes a degree of freedom and forms a diode connection that is no longer adjustable.

Since the programming gate and the control gate in the GeRFET model have a similar effect on the drain current in certain operation regions they are interchangeable to some degree, so we expect a similar behavior

for both connections. A simple current-voltage characteristic of the RFET connected as diode for each configuration is shown and finally compared in Figure 3 to Figure 6.

As shown in Figure 6, the RFET diodes exhibit the same current value at $1.2\ \mathrm{V}$, which is expected since in all 3 cases the voltage of both gates is equal. Below this voltage, the diode configured with adjustable $\mathrm{V_{PG}}$ has the lowest threshold voltage. The notable bump in the CG connected circuit characteristic between $0.8\ \mathrm{V}$ and $0.9\ \mathrm{V}$ is unexpected and the cause of this behavior is currently not known. Otherwise, the behavior when full bias is applied or both gates are tied to drain is comparable to an n-channel MOSFET. For comparison we also added the characteristic curve of an n-FET sized to a similar maximum current (labeled as reference MOSFET).

The adjustability of the circuit can be used to change the voltage-current characteristic of the RFET diode. A higher voltage at the accessible gate results in a higher conduction of the RFET diode and a subsequent reduction in the threshold voltage and a higher slope. This inherent behavior can be used in multiple circuit topologies and will also be exploited in the current mirror circuit in following section 3.3 and 3.4.

As the utilized RFET is almost symmetrical in its p and n-channel characteristic, the diodes can also be used to conduct in the other direction if the sign of the bias voltages is flipped. Since the characteristics are almost identical, when adjusting for the inverted biases, we omitted the graphs for the p-type.

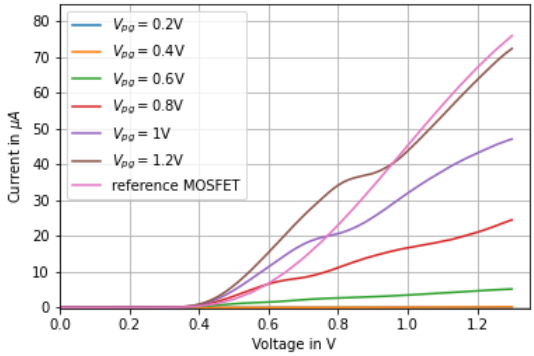

Figure 3: V_{DS}-Voltage vs I_{DS} current of an RFET in diode configuration (V_{PG} adjustable, CG and D connected).

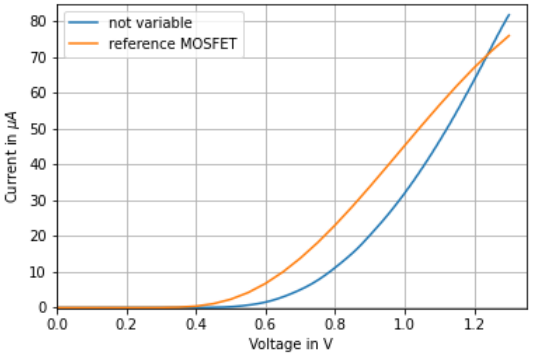

Figure 4: V_{DS}-Voltage vs I_{DS} current of an RFET in diode configuration (not adjustable, CG+PG and D connected).

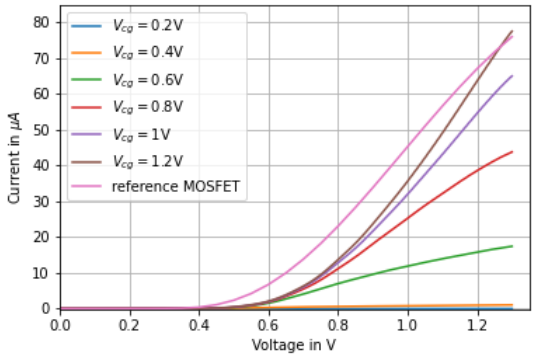

Figure 5: V_{DS}-Voltage vs I_{DS} current of an RFET in diode configuration (V_{CG} adjustable, PG and D connected).

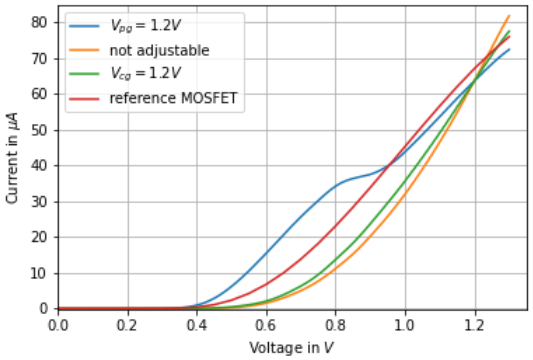

Figure 6: Comparison of the V_{DS}-voltage vs I_{DS} current of an RFET in different diode configurations at a single gate bias.

3. *Common*-Source *Amplifier with Active Load*

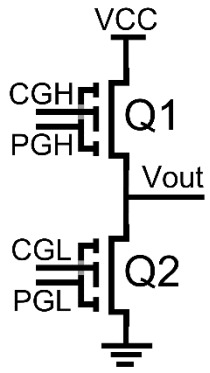

Figure 7: RFET common-source amplifier with active load.

The RFET common-source amplifier with active load is depicted in Figure 7 and utilizes two transistors. One of them can be configured as a quasi-resistor by selecting constant programming and control gate voltages. It is beneficial to choose the biasing in a region where the transistor current is approximately linear over a large range of V_{DS}. These operating regions can be found in the table model of GeRFET e.g. by using linear regression on the V_{DS} sweeps and selecting an operating point with a minimal non-linearity.

In simulations we tested an n-type version of the circuit with $Vcc = 1\,V$, $V_{PGH} = 1\,V$, $V_{CGH} = 0.35\,V$ while V_{PGL} was stepped and V_{CGL} was swept. The DC output voltages of the circuit are shown in Figure 8 at relevant V_{PGL} biases. The gain is highest at approximately $V_{CGL} = 0.14\,V$ and the gain rises with higher V_{PGL} as can be seen in Figure 9. However, the current in this operating region is below $1\,nA$ as can be seen in Figure 10.

Because of the low current drive capability, the output capacitances cannot be charged very quickly. This reduces the bandwidth of this circuit. This low current operating region is interesting nonetheless for low power applications or applications that do not require high bandwidth (e.g. for biomedical applications).

Furthermore, we are working with a device at a fixed W/L ratio. By increasing the width, we expect also higher currents. While a scaling factor in the model is included, it is only based on the simple multiplication of currents since measured or simulated scaling data is not yet available. The current scaling factor was set to one. Another thing to note is that the GeRFET model is based on coarse simulation data. If measurement data or refined simulations is getting available in the future it would be of high interest to do a comparison with the current model and assess if the simulation is accurate in this region.

The RFET version of the common-source amplifier with active load offers great flexibility to the circuit designer, as the gain of the circuit can be adjusted over a wide range, which can be seen in Figure 9. The gain was *extracted* by numerical derivation of the data in Figure 8 and finding the maximum. Additionally, we expect the bandwidth to be tunable as output current can be adjusted. All four gates of the circuit can be used as an input for tuning the device behavior, selecting a DC bias point or even as signal input – which we will discuss in the later part of this document. While this is outside the scope of this document, we could already partially confirm that this characteristic is useful in adjustable gain amplifiers and operational amplifiers and we expect it to be also useful in filters, lock in amplifiers and other circuits.

Furthermore, the circuit can be transformed to its p-type counterpart by flipping all voltages including the supply voltage. The dynamic reconfiguration will be part of a later deliverable and we are looking forward to investigating new circuit ideas based of this principle.

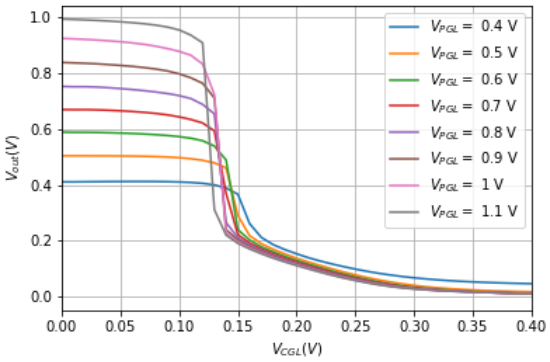

Figure 8: Output voltage of RFET common-source amplifier.

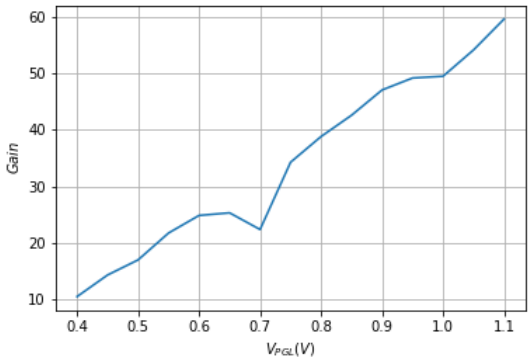

Figure 9: Maximal gain of RFET common-source amplifier.

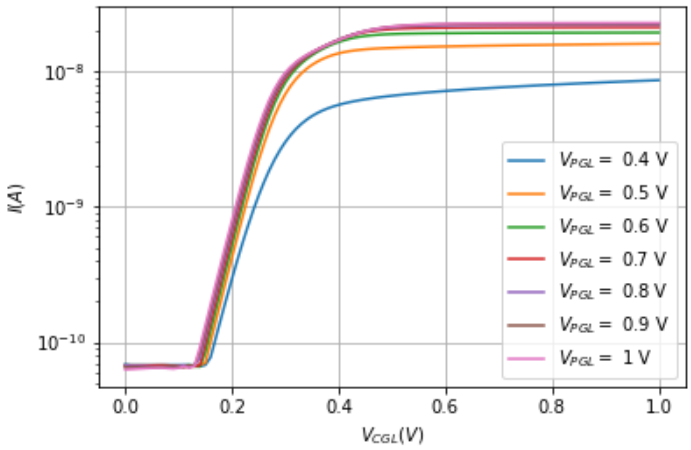

Figure 10: The current in the common-source amplifier can be extremely low.

4. Current *Mirror*

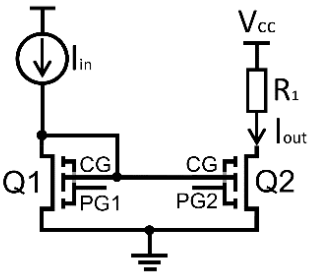

Figure 11: RFET Current Mirror, with resistive load.

The current mirror (Fig. 11) is a basic circuit element that can be found in various circuits. With standard technology the input to output current ratios are fixed by the designer by choosing the transistor sizes accordingly. However, this ratio is prone to errors due to manufacturing tolerances (mismatch).

With RFETs the transfer ratio can be varied by utilizing the programming gates on one of the two transistors (here PG1 or PG2). They can be used to tune the transistor gain and by that to change the input to output ratio, which is not easily archivable with standard CMOS technology. While adjustable current mirror designs in CMOS do exist, they often employ circuits to add additional parallel transistors to the mirror [7], limiting the adjustment to discrete steps. Other adjustable designs are utilizing current steering [8] by injecting a parallel current, which is usually complex and adds additional power consumption. In contrast the RFET is bias voltage controlled and directly changes the transistor properties adding a new possibility for circuit designers as both CMOS strategies could still be added to the RFET circuit.

The described flexibility and analog tunability of the RFET current mirror enable a near perfect realization of a current ratio. This is shown in 2 and 14 where, by applying a correction signal at PG2, to idealize a n-type current mirror to a 1:1 ratio. This is also possible for a p-type mirror which is shown in Figure 13 and Figure 15. The results are based on the GeRFET model with PG1 being held at a constant 0.7 V, $R_1 = 1\ M\Omega$, with $V_{CC} = 0.8\ V$ for the n-channel current mirror and $V_{CC} = -0.8\ V$ for p-channel version. As evident in the figures, the correcting function overall is nonlinear but has flat regions where almost no adjustment is needed. These regions are desirable operating points if the programming gate voltages are constant. In the

future we plan to develop a compensation mechanism that can be implemented together with the RFET current mirrors, to compensate unwanted nonlinearities.

Besides adjustability, RFET current mirrors can switch between p-channel and n-channel configuration, which allows for complete reconfigurability, which we will further research and expect to present as part of the deliverable *D4.2 – Functional Elements Exploiting Dynamic Reconfiguration*.

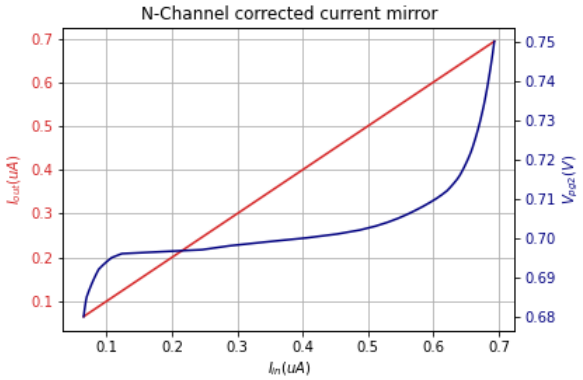

Figure 12: Applied correction bias for n-channel current mirror.

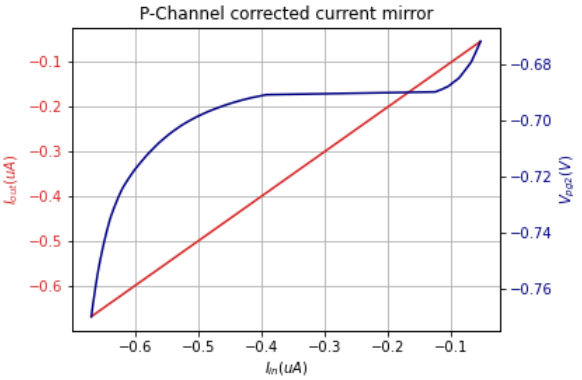

Figure 13: Applied correction bias for p-channel current mirror.

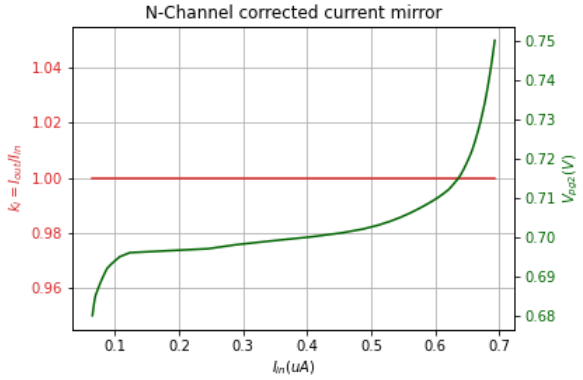

Figure 14: N-Channel corrected current mirror.

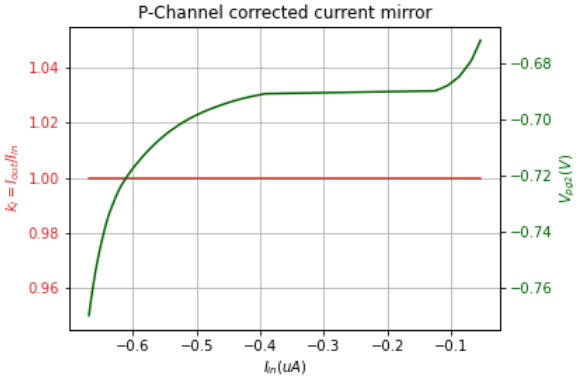

Figure 15: P-Channel corrected current mirror.

5. Differential *Pair*

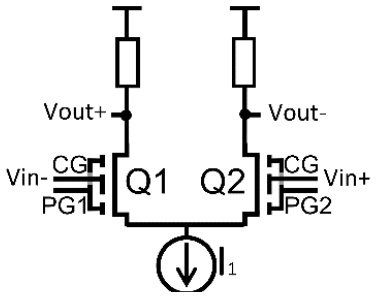

Figure 16: Differential RFET pair.

Next the differential pair circuit (Figure 16) was build from RFETs. The differential pair was tested with ideal static resistors instead of transistors (as in in the common-source circuit) to minimize the influence of choosing a second biasing point for the high side RFETs and an ideal current source for I_1. The gain of this circuit in dependence of the current I_1 is plotted in Figure 17.

As evident the gain increases with the applied current because the ideal current source forces the current through the RFETs. Note that it is important to keep the common source terminals at an acceptable voltage level. Otherwise, the model could be outside the permitted range.

The circuit can be used like a normal differential pair, by applying a constant voltage to the programming gates. If there is a mismatch between the two RFETs like in traditional CMOS circuits the output voltage will have an offset. This mismatch can happen during manufacturing and can never be totally avoided. While in a CMOS circuits the offset is fixed and additional circuits need to be employed to correct the mismatch, in

the RFET circuit this can be compensated by changing the bias voltage at the programming gates. This circuit behavior is illustrated in Figure 18 where an offset is generated in perfectly matched RFETs by changing V_{PG1} while V_{PG2} is kept at a constant $0.7\ V$. While it seems counterintuitive to generate an offset the same principle can be applied in a reverse way, to compensate for an offset.

A high offset voltage can be generated by using high variations in programming gate voltages. The magnitude of the offset is illustrated over the difference in programming gate voltages in Figure 19. Please note that all traces pass through the $0\ V$ offset region when the difference in programming gate voltages is also $0\ V$, since we used a simulation with two ideally matched RFETs in the circuit.

The offset reduction is a useful property of this circuit that shows the inherent functionality of the RFETs used. This behavior will be highly useful in future circuits like operational amplifiers or comparators where it is key to minimize the input offset voltage.

While the difference of the programming gate voltages is important for offset compensation the common absolute value can be used to influence the conductivity of the RFETs. This property should be useful to further adjust the gain and the bandwidth when considering constant capacitances.

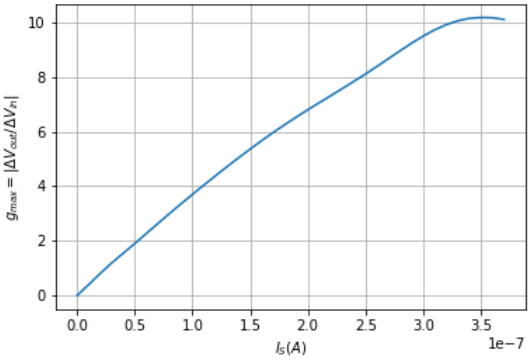

Figure 17: Differential RFET pair gain over current consumption.

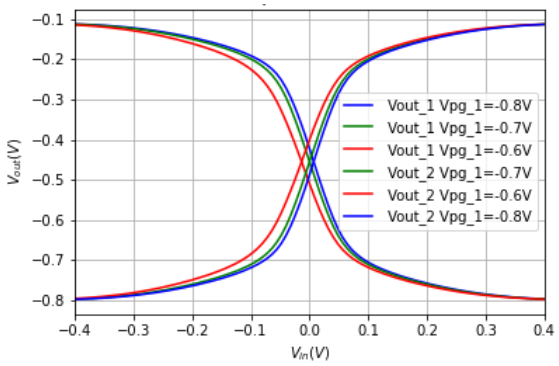

Figure 18: With RFETs the mismatch can be compensated.

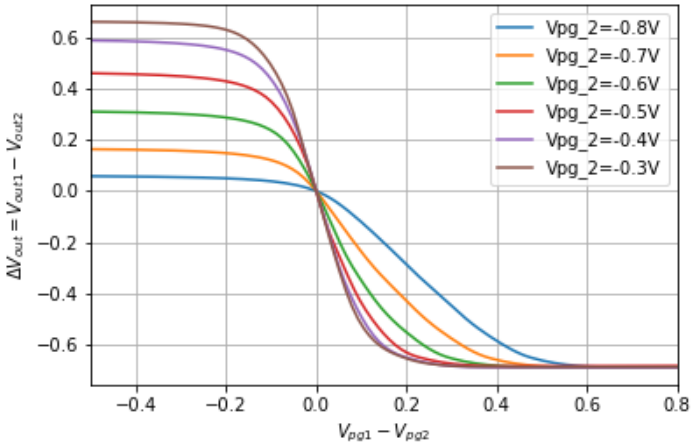

Figure 19: Compensation of offset or mismatch.

Besides the DC simulations transient simulations were also done to show the potential of the RFET differential pair. A transient simulation of the circuit with a sinusoidal input voltage with a frequency of $10\ kHz$ was performed. The results of the simulations are depicted in Figure 20 and clearly show the gain of the circuit. The differential pair circuit also could be used as a mixer circuit. In this configuration a small signal is modulated on the bias voltage of the programming gates, which would subsequently modulate the output voltage.

We are looking forward to testing the bandwidth limits of the differential pair but are currently limited by the validity of some AC models to produce accurate simulations. In the future the differential RFET pair will find application in comparators, operational amplifiers, and more.

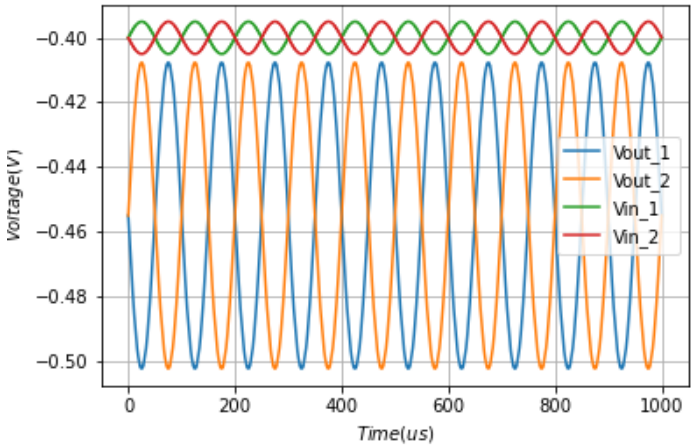

Figure 20: Transient simulation.

6. Mixer

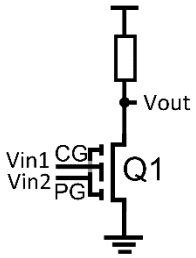

Figure 21: RFET mixer circuit.

The single transistor mixer circuit benefits of an inherent ability of RFETs with at least two gates. Since both gates can modulate the conductance of the device and the device can even switch between majority carrier type. Additionally, small signals on both inputs can be mixed, since both gates can modulate the output.

Figure 22 shows a simulation confirming the expected behavior with a broad range of DC operating points highlighting different achievable modulation types. The simulation was created by applying a $20\,mV_{PP}$ sinus at $1\,kHz$ at the programming gate (V_{PG}) and an DC offset of $450\,mV$. At the same time the control gate (V_{CG}) had a sinus of $10\,kHz$ applied while the DC offset was changed as denoted in the legend.

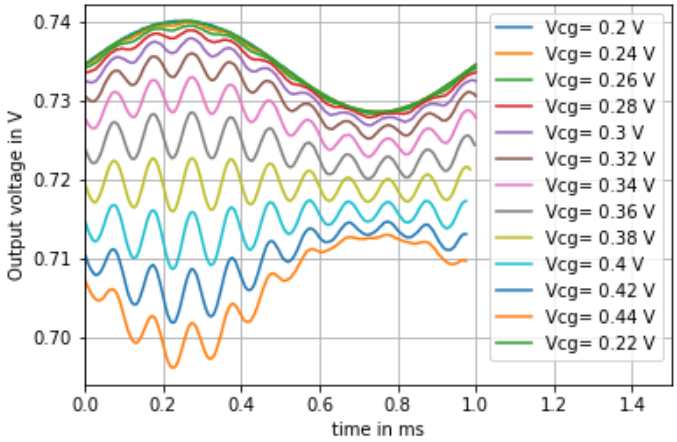

Figure 22: Transient Simulation of the RFET mixer circuit.

By controlling the operating point, we can select the behavior. A low offset voltage at the control gate will transmit the programming gate signal with mostly amplitude alteration to the output. When raising the DC voltage offset the control gate AC signal gets imposed onto the slower programming gate signal. This results in a varying degree of mixed signals that range from the output following the programming gate input (i.e. below $V_{CG} = 0.3\,V$) to the output being an amplitude-modulated version of the control gate signal (i.e. at

$V_{cg} = 0.38\ V$) and finally to an output that inverts the programming gate signal with a slight modulation by the control gate signal (at $V_{CG} = 0.44\ V$). To keep the graphic simple, we choose to fix the programming gate offset to only $450\ mV$. By also varying the programming gate voltage we can achieve inverted signals of the control gate input at the output as well as modulations of the control gate signal as seen above with the programming gate signal.

7. Transmission *Gate*

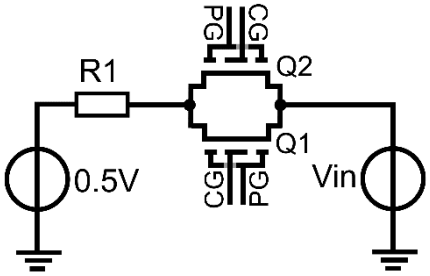

Figure 23: Transmission gate circuit.

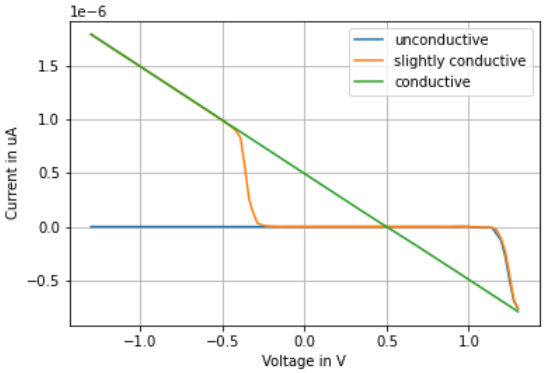

Figure 24: Current through the transmission gate in various conditions.

The transmission gate is a useful circuit that allows currents in both directions to pass if the transmission gate is activated or open. If the transmission gate is deactivated or closed it acts as a high impedance. This circuit is often used in re-routing analog signals for multiplexers.

We simulated an RFET based variant of the circuit. The circuit and the output of the simulation are provided in Figure 23 and Figure 24. The input potential over the transmission gate was swept, while the output was connected to a constant resistor ($R_1 = 1\ M\Omega$) as a load and the output current was recorded. In the plot of the simulation, it is evident that different behaviors exist, which can be categorized in conductive, unconducive, and partially conductive states. The actual behavior depends on the voltage at the control gates and programming gates.

An advantage of the transmission gate is, that it has the same functionality if the sign of all the gate voltages is flipped. By inverting all gate voltages, the transistors are converted from n-channel to p-channel and vice versa. Furthermore, there are intermediate behaviors of the transmission gate that span between conductive and unconducive and that could have useful applications. This includes controlling the conduction state to select an on-resistance. In the future we plan to exploit this behavior and use the transmission gate as a building block in more complex circuits.

4. Summary and Conclusion

Utilizing the available preliminary RFET models developed and provided by several SENSOTERIC project partners [1-5] we could explore multiple interesting circuits employing the inherent higher functionality of RFET devices in analog circuits. We focused our efforts on model evaluation and research on improvements in seemingly simple but fundamental analog integrated circuit building blocks.

The provided DC and rudimentary AC models, which are all implemented in Verilog-A, were successfully integrated into Cadence Virtuoso. Multiple modeling methods were utilized to generate these models, which includes table models, formula-based approaches and AI-models. The models were extensively analyzed to identify their limitations and iteratively work on improvements. It was also necessary to find suitable operating regions for basic circuits since the operating regions are much more complex than traditional CMOS devices.

The findings of these basic circuits can now be used as building blocks for more complex circuits in the future and already have been to some extent. The basic circuits presented in this deliverable include the RFET based diode, common-source amplifier, current mirror, differential pair, mixer and transmission gate and examples of interesting operation abilities are given. Since the modeling effort is still ongoing, we refrained from a numerical analysis and direct comparison to standard CMOS circuit performance and focus on general enhancements.

All presented circuits benefit from the inherent higher functionalities of RFETs, which are their tunability of the I_{DS} current and their full reconfigurability, which relates to switching the transistor from n-type to p-type and vice versa. We found multiple circuit elements that are worth to be investigated further. The findings from these investigations will serve as basis for developing more advanced and complex novel circuit designs in the future.

5. References

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6. Glossary

AC:	Alternating current
CG:	Control Gate
CMOS:	Complementary Metal Oxide Semiconductor
DC:	Direct current
GeRFET:	Germanium Reconfigurable Field Effect Transistor
MOSFET:	Metal Oxide Semiconductor Field Effect Transistor
PG:	Program Gate
RFET:	Reconfigurable Field Effect Transistor
TCAD:	Technology Computer Aided Design
W/L ratio:	Width to Length ratio